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CONFIGURABLE COMPUTERS: THE STATE AND THE FUTURE

Configurable computer is one of the advanced alternatives to the usual computer architectures. Configurable computer is the computer that exchanges its structure at logic and RTL levels during its operation. The first computer ENIAC can be valued as the first configurable computer. Its configuration of connections between registers, accumulators, etc., has been reprogrammed by the exchange of program switchboards.

The configurable computers were investigated and developed successfully in our country at the Lviv Scientific Technical Centrum "Integral" in the period of 1981-1994. They were based on ICs of the homogeneous computing raw, named "Raita", and were used mostly for the image computing.

The high success of the FPGA technology has given a push to the propagation of configurable computers. FPGA can substitute ASICs and supports quick development process and any number of reprogramming cycles. Last decade the gate number, clock frequency and routing capabilities of FPGA grew dramatically. Consider FPGA and microprocessors implement operations like 32-bit multiplication and 64-bit accumulation. Then for every 18 months the throughput of advanced microprocessors and FPGAs grew in 2 times, and in

6 times, respectively, i.e.the FPGAs computational capabilities grew substantially quickly than microprocessor ones.

More than 100 different FPGA boards are developed and are in production now over the world. They are attached to PCs to increase the throughput of them. Many investigations and experiments proved the high effectiveness of these boards. They showed that in many applications one FPGA device has the throughput in one degree of magnitude higher than advanced microprocessor has (in 7-50 times). These applications usually need to be adapted to the architecture that is cardinally different from the microprocessor architecture. They are, for example, bit level computations, data flows with comparing and shuffle, unusual data format handling like multibit integer calculations, etc.

In the configurable computers based on the FPGA board the bottleneck is present which consists in the low througput of the interface between FPGA device and microprocessor.

In the representation an example of new field of using configurable computers is shown. This field is algebraic problem solving, and the example is the Givens QR decomposition. This application is computation intensive and has comparatively low volume of input-output dates. A processor grid is configured in the large Xilinx Virtex FPGA device. These factors help to achieve both high productivity of computer and low needed throughput of the interface. The CORDIC arithmetic used in this application provides the minimum error level when calculating the fixed point numbers. This application was programmed using VHDL language for the Aldec HES-800 FPGA board attached to PC through the PCI interface. Eight

processing units are configured in Virtex-800 device of this board. The total equivalent throughput is estimated as 800 MFLOPS. Both the throughput and the problem dimensions can be increased proportionally by programming larger Virtex devices or by programming a set of devices.

The mentioned above bottleneck can be minimized when the FPGA is placed very close to the microprocessor. This is achieved when both components are placed in the same device. Therefore many FPGA vendors begin the production of devices which contain both FPGA area and microprocessor core. They are Altera Apex with ARM922 and MIPS32 cores, Atmel AT94K with AVR core, Quicklogic QuickMIPSSESP with MIPS32 core, Triscend TE5 with 8051 core, TA7 with ARM7 core, Xilinx VirtexII with PowerPC core.

The modern wireless applications are characterized by the minimized energy consumption, substantially increased throughput and exchanging of computing algorithms and communication protocols. Therefore the configurable computer devices can find the large propagation in the handheld and wireless application market because they can support energy saving, high productivity and quick reprogramming. The MIT Pleyada project of such a device prooves successfully this thesis.

To put configurable computers in life successfully the problem of their programming has to be solved. This problem can be solved in the directions of soft IP core development, hardware-software codesign and development of CADs of system level design. The C-like language compilers adapted to the FPGA architecture can support this process. The example is the CELOXICA compiler.